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(54) [Title of the Invention]
Manufacturing Method of Liquid Crystal Display Panel

(57) [Abstract]

[Problems to be Solved] To manufacture an active matrix drive type liquid crystal display panel of a TFT drive whose light-shielding performance against returning light and transistor characteristics are high.

[Solution] In a manufacturing method of a liquid crystal display panel (100) comprising liquid crystal (50) which is held between a pair of first and second substrates (1 and 2), a pixel electrode provided in a matrix on the first substrate and a

TFT (30) for switching-controlling it, a light-shielding film is formed by sputtering on the first substrate using a WSi target, and the light-shielding film is etched using $SF_6/CF_4/O_2$ as the etching gases.

[Scope of Claims]

[Claim 1] A manufacturing method of a liquid crystal display panel comprising a pair of first and second substrates, liquid crystal held between the first and second substrates, a plurality of transparent pixel electrodes provided in a matrix on a side which faces the liquid crystal of the first substrate, a plurality of switching elements provided on the first substrate in positions adjacent to each of the plurality of pixel electrodes for switching-controlling each of the plurality of pixel electrodes, a light-shielding layer formed of WSi (tungsten silicide) provided between the first substrate and the plurality of switching elements respectively in positions opposing to each of the plurality of switching elements and an interlayer insulating layer provided between the light-shielding layer and the plurality of switching elements, comprising the steps of:

forming a light-shielding film whose thickness is in a range of 1000 Å to 3000 Å on the first substrate by sputtering using a WSi target wherein a mole ratio (Si/W) of Si (silicon) and W (tungsten) is in a range of 2.0 to 3.0 and Si phase grain boundary size is 30 μm or less;

forming a mask which corresponds to a pattern of the light-shielding layer on the formed light-shielding film by photolithography; and

forming the light-shielding layer by performing etching to the light-shielding film through the mask.

[Claim 2] A manufacturing method of a liquid crystal display panel comprising a pair of first and second substrates, liquid crystal held between the first and second substrates, a plurality of transparent pixel electrodes provided in a matrix on a side which faces the liquid crystal of the first substrate, a plurality of switching elements provided on the first substrate in positions adjacent to each of the plurality of pixel electrodes for switching-controlling each of the plurality of pixel electrodes, a light-shielding layer formed of WSi (tungsten silicide) provided between the first substrate and the plurality of switching elements respectively in positions opposing to each of the plurality of switching elements and an interlayer insulating layer provided between the light-shielding layer and the plurality of switching elements, comprising the steps of:

forming a light-shielding film on the first substrate by sputtering using a WSI target;

forming a mask which corresponds to a pattern of the light-shielding layer on the formed light-shielding film by photolithography; and

forming the light-shielding layer by performing chemical dry etching to the light-shielding film through the mask using $SF_6/CF_4/O_2$ as the etching gases, with a flow of SF_6 in a range of 5% to 30% of a flow of all the etching gases, a flow of CF_4 in a range of 30% to 75% of a flow of all the etching gases, and a flow of O_2 in a range of 20% to 40% of a flow of all the etching gases.

[Claim 3] A manufacturing method of a liquid crystal display panel according to claim 1, wherein the etching process comprises the step of performing chemical dry etching using $SF_6/CF_4/O_2$ as the etching gases, with a flow of SF_6 in a range of 5% to 30% of a flow of all the etching gases, a flow of CF_4 in a range of 30% to 75% of a flow of all the etching gases, and a flow of O_2 in a range of 20% to 40% of a flow of all the etching gases.

[Claim 4] A manufacturing method of a liquid crystal display panel according to any one of claims 1 to 3, wherein the liquid crystal display panel is provided further with a wiring formed of WSi having a predetermined wiring pattern, further comprising the steps of:

forming a WSi film for a wiring by sputtering using a WSi target;

forming a mask which corresponds to the wiring pattern on the formed WSi film by photolithography; and

forming the wiring by performing chemical dry etching to the WSi film through the mask using $SF_6/CF_4/O_2$ as the etching gases, with a flow of SF_6 in a range of 5% to 30% of a flow of all the etching gases, a flow of CF_4 in a range of 30% to 75% of a flow of all the etching gases, and a flow of O_2 in a range of 20% to 40% of a flow of all the etching gases.

[Detailed Description of the Invention]

[0001]

[Field of the Invention] The present invention relates to a field of manufacturing method of an active matrix drive type liquid crystal display panel of a TFT (thin film transistor) drive, especially a field of manufacturing method of a liquid crystal display panel provided with a black matrix on the under side of the TFT, used for a liquid crystal projector or the like.

[0002]

[Prior Art] Conventionally, as for a liquid crystal display panel used as a light valve for a liquid crystal projector or the like of this kind, incident light generally is entered from the side of an opposite substrate which is placed opposing to a TFT array substrate with a liquid crystal layer therebetween. Here, when the incident light enters a region for channel formation structured by an a-Si (amorphous silicon) film or a p-Si

(polysilicon) film of the TFT, a photoelectric current is generated by a photoelectric conversion effect in this region, and the transistor characteristics of the TFT deteriorate. Therefore, a plurality of light-shielding layers called black matrix are generally formed in positions which oppose to each TFT on the opposite substrate. Such black matrix is made of a metal material such as Cr (chrome) or a material such as resin black where carbon is dispersed on a photo resist, and it has functions such as improvement of contrast and prevention of color materials mixture, besides light-shielding for the a-Si film and the p-Si film of the TFT mentioned above.

[0003] Furthermore, as for a liquid crystal display panel of this kind, especially in the case where an a-Si or p-Si TFT of a positive stagger type or a coplanar type with a top gate structure (that is, a structure in which a gate electrode is provided on the upper side of the channel) on the TFT array substrate is used, it is necessary to prevent a part of incident light from entering the channel of the TFT from the TFT array substrate side as returning light due to the optical system for projecting in the liquid crystal projector.

[0004] For this reason, in Japanese published unexamined application No. 9-127497 bulletin, Japanese published examined application No. 3-52611 bulletin, Japanese published unexamined application No. 3-125123 bulletin, Japanese published unexamined application No. 8-171101 bulletin and the like, the manufacturing technique of a liquid crystal display panel in which a black matrix is formed also in a position opposing to the TFT (that is, the under side of the TFT) on the TFT array substrate formed of a quartz substrate or the like is proposed. Because of the black matrix formed as this, light-shielding against returning light for the a-Si film or the p-Si film of the TFT is supposed to be possible. Especially according to this manufacturing technique, in order to prevent the black matrix from being destroyed or melting by a high-temperature treatment in the TFT formation process after the black matrix formation process on the TFT array substrate, the black matrix is formed of an opaque refractory metal.

[0005] In addition, according to the conventional manufacturing technique as this, a refractory metal film is formed on the TFT array substrate by sputtering or the like, and after that, the black matrix having a predetermined pattern is formed by etching it.

[0006]

[Problems to be Solved by the Invention] However, according to the conventional manufacturing technique described above, there are following problems. That is, the black matrix for light-shielding against returning light is formed of a refractory metal, so that its thermal compatibility with the TFT array substrate formed of a quartz substrate or the like where the black matrix is formed is bad. More specifically, when

placed in a high-temperature environment and a room temperature environment at the times of process of forming an interlayer insulating layer, a TFT, various electrodes, various wirings and the like over the black matrix after the black matrix is formed and at the time of use, stress is generated due to the difference in physical properties such as coefficient of thermal expansion between the black matrix and the TFT array substrate or each element of these. Therefore, a distortion or a crack occurs in the black matrix, or a distortion or a crack occurs in the TFT array substrate, the interlayer insulating layer, each constituent element of the TFT or the like. Such crack easily occurs in the part where a contact hole for electric connection is formed on each layer, for example. As a result, the formation process of the TFT, the formation process of the wiring and the like do not go well and a conduction failure or an insulation failure occurs, a part of returning light enters a channel of the TFT from the crack of the black matrix in the eventually completed liquid crystal display panel and the transistor characteristics deteriorate, and an image defect due to an element defect occurs.

[0007] In addition, when the black matrix is formed by simply performing etching to the refractory metal film formed on the TFT array substrate by sputtering or the like, as the conventional manufacturing technique described above, the section of the formed black matrix becomes a rectangle or an overhang. Therefore, when a wiring is provided thereon, or a TFT, a pixel electrode or the like is provided above via an interlayer insulating layer therebetween, adhesion of the wiring, the interlayer insulating layer or the like is bad, and as a result, a conduction failure such as disconnection and an insulation failure are caused.

[0008] In this way, according to the conventional manufacturing technique described above, transistor characteristics of the TFT deteriorate by forming the light-shielding film on the under side of the TFT, and conduction, insulation or the like of the TFT, various electrodes formed above and the light-shielding film itself becomes defective by forming the light-shielding film inside of a base, which are problems. Furthermore, there is also a problem that the light-shielding film structured as this is not enough to shield against returning light.

[0009] The present invention is made in view of the above-mentioned problems, and its task is to provide a manufacturing method of a liquid crystal display panel with which an active matrix drive type liquid crystal display panel whose light-shielding performance against light such as returning light from the under side of a switching element such as a TFT and switching characteristics of the switching element are high, by forming a light-shielding layer suppressing the generation of stress due to the difference in coefficient of thermal expansion or the like as described above.

[0010]

[Means for Solving the Problem] In order to solve the above-described problems, the manufacturing method of a liquid crystal display panel according to claim 1 is a manufacturing method of a liquid crystal display panel comprising a pair of first and second substrates, liquid crystal held between the first and second substrates, a plurality of transparent pixel electrodes provided in a matrix on a side which faces the liquid crystal of the first substrate, a plurality of switching elements provided on the first substrate in positions adjacent to each of the plurality of pixel electrodes for switching-controlling each of the plurality of pixel electrodes, a light-shielding layer formed of WSi (tungsten silicide) provided between the first substrate and the plurality of switching elements respectively in positions opposing to each of the plurality of switching elements and an interlayer insulating layer provided between the light-shielding layer and the plurality of switching elements, comprising the steps of: forming a light-shielding film whose thickness is in a range of 1000 Å to 3000 Å on the first substrate by sputtering using a WSi target wherein a mole ratio (Si/W) of Si (silicon) and W (tungsten) is in a range of 2.0 to 3.0 and Si phase grain boundary size is 30 μm or less; forming a mask which corresponds to a pattern of the light-shielding layer on the formed light-shielding film by photolithography; and forming the light-shielding layer by performing etching to the light-shielding film through the mask.

[0011] According to the manufacturing method of a liquid crystal display panel according to claim 1, a light-shielding film is formed on a first substrate by sputtering, a mask which corresponds to a pattern of a light-shielding layer is formed on the light-shielding film by photolithography, and etching is performed to the light-shielding film through the mask, so that the light-shielding layer of a particular pattern is formed.

[0012] Here, especially in the sputtering process, a WSi target is used. As for the WSi target, the mole ratio (Si/W) of Si and W is in a range of 2.0 to 3.0, so the thermal compatibility between the light-shielding layer formed of WSi which is refractory metal silicide including silicon and the first substrate formed of a quartz substrate or the like is good. More specifically, compared to the case where the light-shielding layer is formed of a refractory metal such as W, Ti (titanium), Cr (chrome), Ta (tantalum), Mo (molybdenum) and Pd (lead), the case where the light-shielding layer is formed of silicide of refractory metal such as Ti, Cr, Ta, Mo and Pd, or the case where the light-shielding layer formed of WSi is formed using a WSi target with a mole ratio of less than 2.0 or more than 3.0, stress generated due to the difference in physical properties such as coefficient of thermal expansion between the light-shielding layer and the first substrate, the interlayer insulating layer and each constituent element of the

switching element at the time of being placed in a high-temperature environment and a room temperature environment is decreased. Furthermore, as for the WSi target used in the sputtering process, the Si phase grain boundary size is 30 μm or less, so that homogenization of film quality of the light-shielding layer is promoted. By this, local decrease in light-shielding properties in the light-shielding layer is prevented. On the other hand, the light-shielding layer's performance as a base layer of the switching element improves, and local stress or generation of a crack due to inhomogeneous film quality of the light-shielding layer can be prevented. In addition, since the thickness of the light-shielding film formed as this is 1000 Å or more, light-shielding rate (transmissivity) of 1% or less which is enough light-shielding properties to prevent characteristics of the switching element from deteriorating even when light such as returning light enters the liquid crystal display panel from the first substrate side can be obtained. On the other hand, since the thickness of the light-shielding film is 3000 Å or less, planarization of the upper surface of the light-shielding layer where the interlayer insulating layer is to be formed is promoted, and stress due to the difference in coefficient of thermal expansion or the like described above can be prevented from being excessively increased with the thickness.

[0013] Therefore, light-shielding properties of the light-shielding layer and the switching characteristics of the switching element can be improved, while preventing a distortion or a crack from occurring in the light-shielding layer , or a distortion or a crack from occurring in the first substrate, the interlayer insulating layer, each constituent element of the switching element or the like.

[0014] In order to solve the above-described problems, the manufacturing method of a liquid crystal display panel according to claim 2 is a manufacturing method of a liquid crystal display panel comprising a pair of first and second substrates, liquid crystal held between the first and second substrates, a plurality of transparent pixel electrodes provided in a matrix on a side which faces the liquid crystal of the first substrate, a plurality of switching elements provided on the first substrate in positions adjacent to each of the plurality of pixel electrodes for switching-controlling each of the plurality of pixel electrodes, a light-shielding layer formed of WSi (tungsten silicide) provided between the first substrate and the plurality of switching elements respectively in positions opposing to each of the plurality of switching elements and an interlayer insulating layer provided between the light-shielding layer and the plurality of switching elements, comprising the steps of: forming a light-shielding film on the first substrate by sputtering using a WSi target; forming a mask which corresponds to a pattern of the light-shielding layer on the formed light-shielding film by photolithography; and

forming the light-shielding layer by performing chemical dry etching to the light-shielding film through the mask using $SF_6/CF_4/O_2$ as the etching gases, with a flow of SF_6 in a range of 5% to 30% of a flow of all the etching gases, a flow of CF_4 in a range of 30% to 75% of a flow of all the etching gases, and a flow of O_2 in a range of 20% to 40% of a flow of all the etching gases.

[0015] According to the manufacturing method of a liquid crystal display panel according to claim 2, a light-shielding film is formed on a first substrate by sputtering using a WSi target, a mask which corresponds to a pattern of a light-shielding layer is formed on the light-shielding film by photolithography, and etching is performed to the light-shielding film through the mask, so that the light-shielding layer of a particular pattern is formed.

[0016] Here, especially in the etching process, $SF_6/CF_4/O_2$ are used as the etching gases for the chemical dry etching. And, a flow of SF_6 is set to be in a range of 5% to 30% of a flow of all the etching gases, and a flow of CF_4 is set to be in a range of 30% to 75% of a flow of all the etching gases. In this way, etching can be performed to the light-shielding film in a relatively short time with a practically reasonably high etching rate of approximately several hundred to several thousand Å (angstrom)/min (minutes), for example, keeping uniformity of the etching and selectivity of the etching for the light-shielding layer and the first substrate high enough. In addition to that, since a flow of O_2 is set to be in a range of 20% to 40% of a flow of all the etching gases, the chemical dry etching can be performed so that the light-shielding layer after the etching has a taper without overhanging. As a result, when various wirings or the like such as wirings for an interlayer insulating layer, a switching element, various electrode and a light-shielding layer are formed over the light-shielding layer having a taper as a base, adhesion of the interlayer insulating layer, the wiring or the like is dramatically good, compared to the case where a light-shielding layer in the shape of an overhang or a rectangle is used as a base as in the conventional manufacturing technique described above.

[0017] In order to solve the above-described problems, the manufacturing method of a liquid crystal display panel according to claim 3 is a manufacturing method according to claim 1 wherein the etching process comprises the step of performing chemical dry etching using $SF_6/CF_4/O_2$ as the etching gases, with a flow of SF_6 in a range of 5% to 30% of a flow of all the etching gases, a flow of CF_4 in a range of 30% to 75% of a flow of all the etching gases, and a flow of O_2 in a range of 20% to 40% of a flow of all the etching gases.

[0018] According to the manufacturing method according to claim 3, since the

sputtering process of claim 1 and the etching process of claim 2 are both included, functions and effects of these processes can be both obtained.

[0019] In order to solve the above-described problems, the manufacturing method of a liquid crystal display panel according to claim 4 is a manufacturing method according to any one of claims 1 to 3, wherein the liquid crystal display panel is provided further with a wiring formed of WSi having a predetermined wiring pattern, further comprising the steps of: forming a WSi film for a wiring by sputtering using a WSi target; forming a mask which corresponds to the wiring pattern on the formed WSi film by photolithography; and forming the wiring by performing chemical dry etching to the WSi film through the mask using $SF_6/CF_4/O_2$ as the etching gases, with a flow of SF_6 in a range of 5% to 30% of a flow of all the etching gases, a flow of CF_4 in a range of 30% to 75% of a flow of all the etching gases, and a flow of O_2 in a range of 20% to 40% of a flow of all the etching gases.

[0020] According to the manufacturing method of a liquid crystal display panel according to claim 4, even for a wiring made of WSi such as a gate wiring of the case where a switching element is a TFT, for example, the chemical dry etching can be performed so that the wiring after the etching has a taper, while performing etching for a WSi film for a wiring with a high etching rate, in the same way as the case of the light-shielding film in claim 2 or 3. As a result, when various wirings, an insulating layer, various electrodes or the like are formed over the wiring having a taper as a base, adhesion of these is dramatically good.

[0021] These functions and other benefits of the present invention will become clear from embodiments described below.

[0022]

[Embodiments] Hereinafter, embodiments of the present invention will be described, based on the drawings.

[0023] Fig. 1 is a cross-sectional view of a liquid crystal display panel of an embodiment of the present invention. In Fig. 1, in order to show each layer and each member in a recognizable size on the drawing, different reduction scales are used for each layer and each member. Fig. 2 is a plan view of various electrodes or the like formed on a TFT array substrate 1 shown in Fig. 1.

[0024] In Fig. 1, a liquid crystal display panel 100 is provided with the TFT array substrate 1 which structures an example of a transparent first substrate and an opposite substrate 2 which structures an example of a transparent second substrate placed opposing to the TFT array substrate 1. The TFT array substrate 1 is formed of a quartz substrate, for example, and the opposite substrate 2 is formed of a glass substrate, for

example.

[0025] The TFT array substrate 1 is provided with a plurality of transparent pixel electrodes 11 in a matrix, as shown in Fig. 2, and an orientation film 12 with a predetermined orientation treatment such as a rubbing done is provided thereon, as shown in Fig. 1. The pixel electrode 11 is formed of a transparent conductive thin film such as an ITO film (indium tin oxide film), for example. The orientation film 12 is formed of an organic thin film such as a polyimide thin film, for example.

[0026] On the other hand, the opposite substrate 2 is provided with a common electrode 21 on all over its surface, and an orientation film 22 with a predetermined orientation treatment such as a rubbing done is provided under. The common electrode 21 is formed of a transparent conductive thin film such as an ITO film, for example. The orientation film 22 is formed of an organic thin film such as a polyimide thin film, for example.

[0027] The TFT array substrate 1 is provided with a plurality of TFTs 30 as an example of switching elements for switching-controlling the plurality of pixel electrodes 11 respectively, in positions adjacent to each of the plurality of pixel electrodes 11, as shown in Fig. 1 and Fig. 2.

[0028] The opposite substrate 2 is further provided with a black matrix 23 in a predetermined region opposing to the TFT 30. The black matrix as this is made from a metal material such as Cr (chrome) and Ni (nickel) or a material such as resin black where carbon or Ti (titanium) is dispersed on a photo resist, and it has functions such as improvement of contrast and prevention of color materials mixture, besides light-shielding for the p-Si (polysilicon) layer 32 of the TFT 30.

[0029] Between the TFT array substrate 1 and the opposite substrate 2 which are structured as above and placed so that the pixel electrodes 11 and the common electrodes 21 face each other, a space enclosed by an after-mentioned sealing agent 52 (refer to Fig. 4 and Fig. 5) is filled with liquid crystal, so that a liquid crystal layer 50 is formed. The liquid crystal layer 50 has a predetermined orientation condition by the orientation films 12 and 22, under the condition where an electric field from the pixel electrode 11 is not applied. The liquid crystal layer 50 is formed of liquid crystal mixed with one or several kinds of nematic liquid crystal, for example. The sealing agent 52 is an adhesive to bond the two substrates 1 and 2 in their peripheries.

[0030] In positions opposing to the TFTs 30 respectively, light-shielding layers 3 formed of WSi (tungsten silicide) are provided respectively between the TFT array substrate 1 and the plurality of TFTs 30. Furthermore, a first interlayer insulating layer 41 is provided between the light-shielding layer 3 and the plurality of TFTs 30. The

first interlayer insulating layer 41 is provided for electrically insulating a p-Si layer 32 structuring the TFT 30 from the light-shielding layer 3. Furthermore, the first interlayer insulating layer 41 is formed all over the surface of the TFT array substrate 1 so that it has a function as a base film for the TFT 30. That is, it has a function of preventing the characteristics of the TFT 30 from deteriorating due to roughness at the time of polishing of the TFT array substrate 1's surface, dirt remained after cleaning or the like.

[0031] As for the light-shielding layer 3, in the case where it is formed using the sputtering process in the first example or the third example of the after-mentioned manufacturing process, the bad thermal compatibility between the light-shielding layer 3 and the TFT array substrate 1 is improved, compared to the case where the above-mentioned conventional manufacturing technique (Japanese published unexamined application No. 9-127497 bulletin or the like) is used.

[0032] In addition, as for the light-shielding layer 3, it is formed so as to have a taper in the case where it is formed using the etching process in the second example or the third example of the after-mentioned manufacturing process. Therefore, adhesion of the interlayer insulating layer, the wiring or the like formed above the light-shielding layer 3 is dramatically good, compared to the case where a light-shielding layer in the shape of an overhang or a rectangle is used as a base as in the above-mentioned conventional manufacturing technique (Japanese published unexamined application No. 9-127497 bulletin or the like), and possibility of a conduction failure and an insulation failure between each layer is reduced.

[0033] The light-shielding layer 3 is grounded or connected to a constant potential source, via a predetermined wiring through a contact hole not shown in the figure. In this way, the switching characteristics of the TFT 30 or the like is not badly affected by the change in electric potential of the light-shielding layer 3. However, the light-shielding layer 3 may be electrically floating, or, the light-shielding layer 3 may be used as a wiring for an after-mentioned storage capacitor (refer to Fig. 3).

[0034] The first interlayer insulating layer 41 is formed of highly insulating glass such as NSG (non doped silicate glass), PSG (phosphorus silicate glass), BSG (boron silicate glass), BPSG (boron phosphorus silicate glass) and the like, a silicon oxide film or the like.

[0035] As shown in Fig. 1, the TFT 30 is provided with a gate electrode 31 (scanning electrode), a p-Si layer 32 where a channel is formed by an electric field from the gate electrode 31, a gate insulating layer 33 to insulate the gate electrode 31 and the p-Si layer 32, a source region 34 formed in the p-Si layer 32, a source electrode 35 (signal

electrode), and a drain region 36 formed in the p-Si layer 32. One corresponding electrode of the plurality of pixel electrodes 11 is connected to the drain region 36. As mentioned after, the source region 34 and the drain region 36 are formed by doping n-type or p-type dopant of predetermined concentration to the p-Si layer 32, depending on which channel (n-type or p-type) is to be formed. A TFT with an n-type channel has an advantage that the operation speed is high, and a TFT with a p-type channel has an advantage that the p-type channel is made easily. The source electrode 35 (signal electrode) may be structured by a transparent conductive thin film such as an ITO film in the same way as the pixel electrode 11, or it may be structured by an opaque thin film such as a metal film of Al or the like and metal silicide. In addition, over the gate electrode 31, the gate insulating layer 33 and the first interlayer insulating layer 41, a second interlayer insulating layer 42 where a contact hole 37 leading to the source region 34 and a contact hole 38 leading to the drain region 36 are formed respectively is formed. The source electrode 35 (signal electrode) is electrically connected to the source region 34 through this contact hole 37 leading to the source region 34. Furthermore, over the source electrode 35 (signal electrode) and the second insulating layer 42, a third interlayer insulating layer 43 where a contact hole 38 leading to the drain region 36 is formed is formed. The pixel electrode 11 is electrically connected to the drain region 36 through this contact hole 38 leading to the drain region 36. The above-mentioned pixel electrode 11 is provided on the upper surface of the third interlayer insulating layer 43 structured as this.

[0036] Here, when light enters the p-Si layer 32 where a channel is formed, a photoelectric current is generated by a photoelectric conversion effect which p-Si has, and the transistor characteristics of the TFT 30 deteriorate, generally. However, in the present embodiment, a plurality of black matrixes 23 are formed in positions opposing to each TFT 30 on the opposite substrate 2, so incident light is prevented from entering the p-Si layer 32 directly. In addition to that, or in place of that, when the source electrode 35 (signal electrode) is formed of an opaque metal thin film such as Al so as to cover the gate electrode 31 from the upper side, it can effectively prevent incident light (that is, light from the upper side in Fig. 1) from entering the p-Si layer 32, with the black matrix 23 or by itself.

[0037] As shown in the plan view of Fig. 2, the pixel electrodes 11 structured as above are arranged in a matrix on the TFT array substrate 1, and the TFT 30 is provided adjacent to each pixel electrode 11. In addition, the source electrode 35 (signal electrode) and the gate electrode 31 (scanning electrode) are provided along the horizontal and vertical borders of the pixel electrode 11 respectively. Fig. 2 is to show

the matrix arrangement of the pixel electrodes 11 and the like, simplifying them for convenience of explanation. Each of the actual electrodes is wired between or on the interlayer insulating layers through contact holes or the like, and it has a three-dimensional, more complex structure as can be seen in Fig. 1.

[0038] Although not shown in Fig. 1, a storage capacitor 70 is provided for the pixel electrode 11 respectively, as shown in Fig. 3. More specifically, this storage capacitor 70 is structured by a p-Si layer 32' formed by the same process as the p-Si layer 32, an insulating layer 33' formed by the same process as the gate insulating layer 33, a storage capacitor electrode (capacity line) 31' formed by the same process as the gate electrode 31, the second and third interlayer insulating layers 42 and 43, and a part of the pixel electrode 11 opposing to the storage capacitor electrode 31' through the second and third interlayer insulating layers 42 and 43. Since the storage capacitor 70 is provided as this, a highly-detailed display is possible even when the duty ratio is small. As shown in Fig. 2, the storage capacitor electrode (capacity line) 31' is provided so as to be parallel to the gate electrode (scanning electrode) 31 on the surface of the TFT array substrate 1. Furthermore, as described above, the light-shielding layer 3 may be used as a wiring for the storage capacitor 70.

[0039] The entire structure of the liquid crystal display panel 100 structured as above will be described, referring to Fig. 4 and Fig. 5. Fig. 4 is a plan view in which the TFT array substrate 1 and each constituent element formed thereon are seen from the opposite substrate 2 side, and Fig. 5 is a cross-sectional view at H-H' of Fig. 4, showing the opposite substrate 2 included.

[0040] In Fig. 4, on the TFT array substrate 1, a sealing agent 52 is provided along the edge, and a periphery break line 53 of the opposite substrate 2 is set in parallel on the inside. In a region outside of the sealing agent 52, a driver circuit for X-side drive 101 and a mounting terminal 102 are provided along one side of the TFT array substrate 1, and driver circuits for Y-side drive 104 are provided along the two sides adjacent to the one side described above. A plurality of wirings 105 are provided on the last one side of the TFT array substrate 1. In addition, silver points 106 formed of a conduction agent to obtain electric continuity between the TFT array substrate 1 and the opposite substrate 2 are provided in the four corners of the sealing agent 52. And, as shown in Fig. 5, the opposite substrate 2 having substantially the same contour as the sealing agent 52 shown in Fig. 4 is bonded to the TFT array substrate 1 by the sealing agent 52.

[0041] The driver circuit for X-side drive 101 and the driver circuit for Y-side drive 104 are electrically connected to the source electrode 35 (signal electrode) and the gate electrode (scanning electrode) by wirings respectively. A display signal converted to a

form with which an immediate display is possible is inputted to the driver circuit for X-side drive 101 from a control circuit not shown in the figure, and the driver circuit for X-side drive 101 sends a signal voltage corresponding to the display signal to the source electrode 35 (signal electrode), in accordance with the driver circuit for Y-side drive 104 sending a gate voltage to the gate electrode 31 (scanning electrode) in order, like a pulse. Especially in the present embodiment, the TFT 30 is a TFT of a p-Si (polysilicon) type, so it is possible that the driver circuit for X-side drive 101 and the driver circuit for Y-side drive 104 are formed in the same process when the TFT 30 is formed, which is advantageous in manufacturing.

[0042] Instead of providing the driver circuit for X-side drive 101 and the driver circuit for Y-side drive 104 on the TFT array substrate 1, they may be electrically and mechanically connected to an LSI for drive which is mounted on a TAB (tape automated bonding substrate), for example, through an anisotropic conductive film provided on the peripheral part of the TFT array substrate 1.

[0043] Furthermore, although not shown in Fig. 1 to Fig. 5, a polarizing film, a phase difference film, an polarizing plate and the like are placed in a predetermined direction on the side where incident light enters of the opposite substrate 2 and on the side from where incident light exits of the TFT array substrate 1 respectively, corresponding to the operation mode such as a TN (twisted nematic) mode, STN (super TN) mode and D-STN (double-STN) mode, or the difference of a normally white mode and a normally black mode, for example.

[0044] Next, the operation of the present embodiment structured as above will be described, referring to Fig. 1 to Fig. 5.

[0045] First, the driver circuit for X-side drive 101 which received a display signal from the control circuit applies a signal voltage to the source electrode 35 (signal electrode), with the timing and size corresponding to this display signal. In parallel with this, the driver circuit for Y-side drive 104 sequentially applies a gate voltage to the electrode 31 (scanning electrode) with a predetermined timing, like a pulse, and the TFT 30 is driven. By this, in the TFT 30 to which a source voltage is applied when the gate voltage is on, a voltage is applied to the pixel electrode 11 through the source region 34, the channel and drain region 36 formed in and the p-Si layer 32. And, the voltage of the pixel electrode 11 is maintained by the storage capacitor 70 (refer to Fig. 3) for a triple-digits longer time, for example, than the time the source voltage is applied.

[0046] In this way, when a voltage is applied to the pixel electrode 11, the orientation condition of liquid crystal in a part held between the pixel electrode 11 and the common electrode 21 in the liquid crystal layer 50 changes. In the case of the normally white

mode, the incident light cannot pass through the liquid crystal part under the condition where the voltage is applied, and in the case of the normally black mode, the incident light can pass through the liquid crystal part under the condition where the voltage is applied. And as a whole, light having a contrast corresponding to the display signal is emitted from the liquid crystal display panel 100.

[0047] Especially in the present embodiment, the light-shielding layer 3 is provided under the TFT 30, so that bad effects due to returning light are reduced, as described above. Therefore, the transistor characteristics of the TFT 30 are improved, and ultimately, a well-colored, high-quality image with a high contrast can be displayed by the liquid crystal display panel 100.

[0048] <First example of the manufacturing process> Next, the first example of the manufacturing process of a liquid crystal display panel 100 will be described, referring to Fig. 6 and Fig. 7.

[0049] First, as shown in the process (1) of Fig. 6, a TFT array substrate 1 of a quartz substrate, hard glass or the like is prepared. Here, an annealing treatment is performed preferably with an inert gas atmosphere such as N_2 (nitrogen) and high temperature of approximately 1000 °C, and a pretreatment for reducing a distortion generated in the TFT array substrate 1 in the high temperature process conducted later is performed.

[0050] A light-shielding film is formed all over the surface of the TFT array substrate 1 treated as above, by sputtering using a WSi target. Then, a mask which corresponds to a pattern of the light-shielding layer 3 is formed on the formed light-shielding film by photolithography. And by performing etching to the light-shielding film through the mask, the light-shielding film formed all over the substrate surface is left only in a region where a TFT 30 is to be formed, so that the light-shielding layer 3 is formed.

[0051] Especially in the first example of the manufacturing process, in the sputtering process, the mole ratio (Si/W) of Si (silicon) and W (tungsten) of the WSi target is in a range of 2.0 to 3.0, and the Si phase grain boundary size is 30 μm or less. And sputtering is performed so that the thickness of the light-shielding film is in a range of 1000 Å to 3000 Å. Here, since the mole ratio (Si/W) of Si and W of the WSi target is in a range of 2.0 to and 3.0, the thermal compatibility between the light-shielding layer 3 formed of WSi which is refractory metal silicide including silicon and the TFT array substrate 1 formed of a quartz substrate including Si or the like is good. More specifically, compared to the case where the light-shielding layer 3 is formed of a refractory metal such as W, Ti, Cr, Ta, Mo and Pd, the case where the light-shielding layer 3 is formed of silicide of refractory metal such as Ti, Cr, Ta, Mo and Pd, and the case where the light-shielding layer formed of WSi is formed using a WSi target with

the mole ratio (Si/W) of less than 2.0 or more than 3.0, stress generated due to the difference in physical properties such as coefficient of thermal expansion between the light-shielding layer 3 and the TFT array substrate 1, the first interlayer insulating layer 41 and each constituent element of the TFT 30 at the time of being placed in a high-temperature environment and a room temperature environment is decreased. Furthermore, as for the WSi target, the Si phase grain boundary size is 30 μm or less, so that homogenization of film quality of the light-shielding layer 3 is promoted. By this, local decrease in light-shielding rate in the light-shielding layer 3 is prevented. On the other hand, the light-shielding layer 3's performance as a base layer of the TFT 30 improves, and local stress or generation of a crack due to inhomogeneous film quality of the light-shielding layer 3 can be prevented. In addition, since the thickness of the light-shielding layer 3 formed as this is 1000 Å or more, light-shielding rate (transmissivity) of 1% or less which is an enough light-shielding properties to prevent characteristics of the TFT 30 from deteriorating even when returning light enters the liquid crystal display panel 100 from the TFT array 1 side can be obtained. On the other hand, since the thickness of the light-shielding layer 3 is 3000 Å or less, planarization of the upper surface of the light-shielding layer 3 where the first interlayer insulating layer 41 is to be formed is promoted, and thermal stress to the light-shielding layer 3 can be prevented from being excessively increased with the thickness. In the case where the light-shielding layer is thinner than 1000 Å, an enough ligh-shielding effect (transmissivity of approximately 1%, for example) cannot be obtained. And in the case where the light-shielding layer is thicker than 3000 Å, thermal stress generated in a high-temperature environment and a room temperature environment in the process of forming the TFT 30 becomes too large. In addition to that, increase in the time and cost for forming the light-shielding layer 3 itself is caused, and a bump of the first interlayer insulating layer 41 on which the TFT 30 is formed later becomes too big, which makes formation of the TFT 30 difficult. It is preferable that the thickness of the light-shielding layer 3 is approximately 1500 to 2500 Å. With this range, good light shielding properties can be obtained, and the problem of a bump hardly occurs practically. As a result of the above, a distortion and a crack in the light-shielding layer 3, or a distortion and a crack in the TFT array substrate 1, the first interlayer insulating layer 41, each constituent element of the TFT 30 or the like can be prevented.

[0052] In addition, when the sputtering process described above is performed, it is preferable that the temperature of the TFT transistor substrate 1 is kept at approximately 200 °C. When the sputtering is performed as this, generation of thermal stress to the light-shielding layer 3 can be decreased without virtually raising the transmissivity of

the light-shielding layer 3 (that is, without virtually decreasing light-shielding effect).

[0053] The light-shielding layer 3 is formed so as to cover at least a region for channel formation, the source region 34 and the drain region 36 of the p-Si layer 32 of the TFT 30, seen from the rear surface of the TFT array substrate 1.

[0054] Next, as shown in the process (2) of Fig. 6, the first interlayer insulating layer 41 formed of a silicate glass film such as NSG, PSG, BSG and BPSG, a nitride film, a silicon oxide film or the like is formed on the light-shielding layer 3 by atmospheric or low pressure CVD or the like, using TEOS (tetraethyl orthosilicate) gas, TEB (triethoxy borine) gas, TMOP (trimethoxy phosphine) gas or the like. It is preferable that the thickness of the first interlayer insulating layer 41 is approximately 500 to 8000 Å. Or, a high-temperature oxidized silicon film (HTO film) or a nitride film may be deposited to a relatively thin thickness of approximately 500 Å by low pressure CVD or the like, after a thermally-oxidized film is formed, so that a first interlayer insulating layer 41 having a multilayer structure with a thickness of approximately 2000 Å is formed. In addition, over the silicate glass film as this or in place of it, a plane film may be formed by spin-coating SOG (spin on glass) or conducting a CMP (Chemical Mechanical Polishing) treatment. In this way, when the upper surface of the first interlayer insulating layer 41 has been planarized by spin-coating or a CMP treatment, the TFT 30 can be easily formed thereon later, which is an advantage.

[0055] By conducting an annealing treatment at approximately 900 °C to the first interlayer insulating layer 41, it may be planarized as well as preventing contamination.

[0056] Next, as shown in the process (3) of Fig. 6, an a-Si (amorphous silicon) film is formed on the first interlayer insulating layer 41 by low pressure CVD (CVD with a pressure of approximately 20 to 40 Pa, for example) using a silane gas, a disilane gas or the like with the flow approximately 400 to 600 cc/min, in a relatively low temperature environment of approximately 450 to 550 °C, preferably approximately 500 °C. After that, a p-Si (polysilicon) film is grown in a solid phase to a thickness of approximately 500 to 2000 Å, preferably to a thickness of approximately 1000 Å, by conducting an annealing treatment for approximately 1 to 10 hours, preferably 4 to 6 hours, at approximately 600 to 700 °C, in a nitrogen atmosphere. At this time, in the case of making a TFT 30 of an n-channel type, a small amount of dopant of V group element such as Sb (antimony), As (arsenic) and P (phosphorus) is doped by ion implantation or the like. Furthermore, in the case where a TFT 30 is to be a p-channel type, a small amount of dopant of III group element such as Al (aluminum), B (boron), Ga (gallium) and In (indium) is doped by ion implantation or the like. A p-Si film may be directly formed by low pressure CVD or the like, without going through an a-Si film. Or,

silicon ions may be implanted to a p-Si film deposited by low pressure CVD or the like to make it amorphous once, then it may be recrystallized by an annealing treatment or the like so that a p-Si film is formed.

[0057] Next, as shown in the process (4) of Fig. 6, a thermally-oxidized film with a relatively thin thickness of approximately 300 Å is formed by thermally oxidizing the p-Si layer 32 at a temperature of approximately 900 to 1300 °C, preferably at a temperature of approximately 1000 °C, and a high-temperature oxidized silicon film (HTO film) or a nitride film is deposited to a relatively thin thickness of approximately 500 Å by low pressure CVD or the like, so that a gate insulating layer 33 having a multilayer structure is formed. As a result, the thickness of the p-Si layer 32 becomes approximately 300 to 1500 Å, preferably approximately 350 to 450 Å, and the thickness of the gate insulating layer 33 becomes approximately 200 to 1500 Å, preferably approximately 300 Å. In this way, by shortening the time for high temperature thermal oxidation, warpage due to heat can be prevented in the case of using a large wafer of approximately 8 inches, especially. However, a gate insulating layer 33 having a single layer structure may be formed by only thermally oxidizing the p-Si layer 32.

[0058] Next, as shown in the process (5) of Fig. 6, after p-Si is deposited over the p-Si layer 32 through the gate insulating layer 33 by low pressure CVD or the like, a gate electrode 31 (scanning electrode) is formed by a photolithography process or an etching process using a gate mask.

[0059] However, the gate electrode 31 (scanning electrode) may be formed from a metal film such as Al or a metal silicide film, instead of a p-Si layer. Or it may be formed to be multilayered, combining these metal film or metal silicide film and a p-Si film. In that case, when the gate electrode 31 (scanning electrode) is placed as a light-shielding film corresponding to a part of or all the region covered by a black matrix 23, it is possible that a part of or all the black matrix 23 is omitted, because of the light-shielding properties which the metal film or the metal silicide film has. In that case, especially, decrease in a pixel aperture ratio caused by bonding misalignment of the opposite substrate 2 and the TFT array substrate 1 can be prevented, which is an advantage.

[0060] Next, as shown in the process (6) of Fig. 7, in the case where a TFT 30 is an n-channel type TFT having a LDD (Lightly Doped Drain Structure) structure, in order to form a low concentration dope region which constitutes a part adjacent to the channel side in a source region 34 and a drain region 36 respectively, a dopant of V group element such as P is doped with a low concentration (P ions with a doze amount of 1 to $3 \times 10^{13}/cm^2$, for example) using the gate electrode 31 as a diffusion mask. Next, after

a resist layer is formed on the gate electrode 31 with a mask wider than the gate electrode 31, a dopant of V group element such as P is doped with a high concentration (P ions with a doze amount of 1 to 3 × $10^{15}/cm^2$, for example) as the above. In addition, in the case where a TFT 30 is a p-channel type, in order to form a source region 34 and a drain region 36 in an n-type p-Si layer 32, doping is performed using a dopant of III group element such as B. In the case of an LDD structure as this, an advantage in which a short channel effect can be reduced is obtained. Doping is not necessarily performed divided into two stages for a high concentration and a low concentration like this. For example, a TFT of an offset structure may be made without performing doping of a low concentration, and a TFT of a self-aligning type may be made by an ion implantation technique using P ions, B ions and the like, with the gate electrode 31 as a mask.

[0061] In parallel to these processes, a driver circuit for X-side drive 101 and a driver circuit for Y-side drive 104, having a CMOS (complementary MOS) structure constituted by an n-channel type p-Si TFT and a p-channel type p-Si TFT, are formed in a peripheral part on the TFT array substrate 1. In this way, since the TFT 30 is a p-Si TFT, the driver circuit for X-side drive 101 and the driver circuit for Y-side drive 104 can be formed by the same process when the TFT 30 is formed, which is an advantage in manufacturing.

[0062] Next, as shown in the process (7) of Fig. 7, a second interlayer insulating layer 42 formed of a silicate glass film such as NSG, PSG, BSG and BPSG, a nitride film, a silicon oxide film or the like is formed so as to cover the gate electrode 31 (scanning electrode) by using atmospheric or low pressure CVD, TEOS gas and the like. It is preferable that the thickness of the second interlayer insulating layer 42 is approximately 5000 to 15000 Å. After an annealing treatment at approximately 1000 °C is performed for approximately 20 minutes in order to activate the source region 34 and the drain region 36, a contact hole 37 for a source electrode 31 (signal electrode) is formed by dry etching such as reactive etching and reactive ion beam etching. At this time, when the contact hole 37 is opened by anisotropic etching such as reactive etching and reactive ion beam etching, the aperture shape can be substantially the same as the mask shape, which is an advantage. However, when the aperture is made combining dry etching and wet etching, the contact hole 37 can be a tapered-shape, so that an advantage of preventing breaking at the time of wiring connection can be obtained. In addition, a contact hole to connect the gate electrode 31 (scanning electrode) with a wiring not shown in the figure is also made in the second interlayer insulating layer 42 by the same process as the contact hole 37.

[0063] Next, as shown in the process (8) of Fig. 7, low resistance metal such as Al, metal silicide or the like is deposited on the second interlayer insulating layer 42 to a thickness of approximately 1000 to 5000 Å by sputtering or the like. Then, a source electrode 35 (signal electrode) is formed by a photolithography process, a wet etching process or the like.

[0064] In that case, when the source electrode 35 (signal electrode) is placed as a light-shielding film corresponding to a part of or all the region covered by the black matrix 23, it is possible that a part of or all the black matrix 23 is omitted, because of the light-shielding properties which the metal film such as Al or the metal silicide film has. In that case, especially, decrease in a pixel aperture ratio caused by bonding misalignment of the opposite substrate 2 and the TFT array substrate 1 can be prevented, which is an advantage.

[0065] Next, as shown in the process (9) of Fig. 7, a third interlayer insulating layer 43 formed of a silicate glass film such as NSG, PSG, BSG and BPSG, a nitride film, a silicon oxide film or the like is formed so as to cover the source electrode 35 (signal electrode) by using atmospheric or low pressure CVD, TEOS gas and the like. It is preferable that the thickness of the third interlayer insulating layer 43 is approximately 5000 to 15000 Å. Alternatively, in place of the silicate glass film as this or over it, a plane film may be formed by spin-coating an organic film or SOG (spin on glass), or by conducting a CMP treatment.

[0066] In addition, a contact hole 38 for electrically connecting the pixel electrode 11 and the drain region 36 is formed by dry etching such as reactive etching and reactive ion beam etching. At this time, when the contact hole 38 is opened by anisotropic etching such as reactive etching and reactive ion beam etching, the aperture shape can be substantially the same as the mask shape, which is an advantage. However, when the aperture is made combining dry etching and wet etching, the contact hole 38 can be a tapered-shape, so that an advantage of preventing breaking at the time of wiring connection can be obtained.

[0067] Next, as shown in the process (10) of Fig. 7, a transparent conductive thin film such as an ITO film is deposited to a thickness of approximately 500 to 2000 Å on the third interlayer insulating layer 43 by a sputtering treatment or the like, and the pixel electrode 11 is formed by a photolithography process, a wet etching process or the like. In the case where the liquid crystal display panel 100 is used for a reflective liquid crystal display device, the pixel electrode 11 may be formed from an opaque material with high reflectivity such as Al.

[0068] Then, after an embrocation of an orientation film of polyimide is applied on

the pixel electrode 11, an orientation film 12 shown in Fig. 1 is formed by performing a rubbing treatment in a predetermined direction so that it will have a predetermined pretilt angle.

[0069] On the other hand, as for the opposite substrate 2 shown in Fig. 1, a glass substrate or the like is prepared first, and a black matrix 23 is formed thereon in a position which corresponds to each of the plurality of TFTs 30 through a photolithography process and an etching process after chromium metal is sputtered, for example. The black matrix may be formed from a material such as resin black where carbon or Ti is dispersed on a photo resist, besides a metal material such as Cr and Ni. After that, a transparent conductive thin film such as ITO is deposited to a thickness of approximately 500 to 2000 Å all over the surface of the opposite substrate 2 by a sputtering treatment or the like so that a common electrode 21 is formed. Furthermore, after an embrocation of an orientation film of polyimide is applied on all over the surface of the common electrode 21, an orientation film 22 is formed by performing a rubbing treatment in a predetermined direction so that it will have a predetermined pretilt angle.

[0070] Lastly, the TFT array substrate 1 and the opposite substrate 2 where each layer is formed as described above are bonded together by a sealing agent 52 so that the orientation films 12 and 22 face each other, and liquid crystal formed by mixing a plurality of kinds of nematic liquid crystal, for example, is introduced into a space between the two substrates by vacuum suction or the like, so that a liquid crystal layer 50 of a predetermined thickness is formed.

[0071] As for the storage capacitor 70 shown in Fig. 3, it can be formed as follows: a p-Si layer 32' is formed on the first interlayer insulating layer 41 by the same process as the above-described p-Si layer 32, and an insulating layer 33' is formed thereon by the same process as the above-described gate insulating layer 33, then a storage capacitor electrode (capacity line) 31' is formed thereon by the same process as the gate electrode 31.

[0072] By the manufacturing process above, the liquid crystal display panel 100 shown in Fig. 1 is completed.

[0073] According to this manufacturing process, even in the case of being placed in a high-temperature environment and a room temperature environment, stress generated due to the difference in physical properties such as coefficient of thermal expansion between the light-shielding layer 3 and the TFT array substrate 1 or the first interlayer insulating layer 41 is decreased. Therefore, generation of a distortion and a crack in the light-shielding layer 3, or generation of a distortion and a crack in the TFT array

substrate 1, the first interlayer insulating layer 41, each constituent element of the TFT 30 or the like can be prevented considerably well, compared to the case where the above-mentioned conventional manufacturing technique (Japanese published unexamined application No. 9-127497 bulletin or the like) is used. So, a part of returning light is prevented effectively from entering a channel of the TFT 30 from a crack of the light-shielding layer 3, and also bad effects due to a distortion and a crack of the light-shielding layer 3 or the like on the formation process of the TFT after that can be effectively prevented. As a result, the light-shielding properties and reliability of the light-shielding layer 3 become dramatically better, so that the transistor characteristics of the TFT 30 can be improved.

[0074] As a result of the above, by the first example of the present manufacturing process, the liquid crystal display panel 100 which can display a well-colored, high-definition image with a high contrast can be manufactured relatively easily.

[0075] <Second example of the manufacturing process> Next, the second example of the manufacturing process of a liquid crystal display panel 100 will be described, referring to Fig. 6 to Fig. 11.

[0076] First, in the same way as the first example, a TFT array substrate 1 of a quartz substrate, hard glass or the like is prepared, as shown in the process (1) of Fig. 6.

[0077] Next, a light-shielding film is formed all over the surface of the TFT array substrate 1 by sputtering using a WSi target. Then, a mask which corresponds to a pattern of the light-shielding layer 3 is formed on the formed light-shielding film by photolithography. And by performing etching to the light-shielding film through the mask, the light-shielding film formed all over the substrate surface is left only in a region where a TFT 30 is to be formed, so that the light-shielding layer 3 is formed.

[0078] In the second example of the manufacturing process, especially in the etching process, $SF_6/CF_4/O_2$ are used as the etching gases for the chemical dry etching. And, a flow of SF_6 is set to be in a range of 5% to 30% of a flow of all the etching gases, a flow of CF_4 is set to be in a range of 30% to 75% of a flow of all the etching gases, and a flow of O_2 is set to be in a range of 20% to 40% of a flow of all the etching gases. In this way, etching can be performed to the light-shielding film in a relatively short time with a practically reasonably high etching rate of approximately several hundred to several thousand Å/min, for example. In addition, after the etching, the light-shielding film 3 can be formed so as to have a taper as a light-shielding layer 3b in Fig. 8 (that is, the taper angle is less than 90 degrees), without being an overhang as a light-shielding layer 3' in Fig. 8 (that is, the taper angle is more than 90 degrees) or a rectangle not having a taper as a light-shielding layer 3a in Fig. 8 (that is, the taper angle is 90

degrees), by the chemical dry etching. In Fig. 8, masks 4', 4a and 4b made by a photo resist is indicated by dotted lines in the way of masking corresponding light-shielding layers 3', 3a and 3b.

[0079] Here, the etching gas having such flow ratio will be described in more derail, referring to Fig. 8 to Fig. 11. Fig. 9 shows change in the etching rate and uniformity of the etching rate (uniformity of the etching rate in an 8-inch substrate surface) when a flow of SF_6 in the etching gas formed of $SF_6/CF_4/O_2$ is changed for a light-shielding film formed of WSi. Fig. 10 shows change in the etching rate when a flow of SF_6 in the etching gas formed of $SF_6/CF_4/O_2$ is changed for a quartz substrate as an example of a TFT array substrate 1. Fig. 11 shows change in the etching rate and change in the taper angle when a flow of O_2 in the etching gas formed of $SF_6/CF_4/O_2$ is changed for a light-shielding film formed of WSi.

[0080] First, as seen in Fig. 9, when a flow of SF_6 is increased, the etching rate for a light-shielding film formed of WSi increases, substantially in direct proportion to this. Therefore, according to the conventional idea, high etching rate is obtained by setting a flow of SF_6 high to the extent that the etching depth can be controlled.

[0081] Furthermore, as seen in Fig. 11, when a flow of O_2 is increased, the etching rate increases, substantially in direct proportion to this, up to approximately 10%. And the etching rate is substantially saturated with approximately 10%. Therefore, according to the conventional idea, high etching rate is obtained by setting a flow of O_2 at approximately 10% or a predetermined value less than that to the extent that the etching depth can be controlled.

[0082] However, as seen in Fig. 9, uniformity of the etching rate has the lowest value around a flow of SF_6 10% (that is, the uniformity is best there). In addition, as seen in Fig. 10, when a flow of SF_6 is increased, the etching rate for a quartz substrate increases, substantially in direct proportion to this.

[0083] So, in the present embodiment, a flow of SF_6 is set to be in a range of 5% to 30% of a flow of all the etching gases so that uniformity of the etching rate is lower than 15% with which experientially preferable etching is possible and the selectivity of the etching to the light-shielding film and the quartz substrate is kept high.

[0084] Furthermore, as shown in Fig. 11, when a flow of O_2 is increased, the mask 4' or 4a formed of a photo resist shown in Fig. 8 is hardly etched by the etching up to 15%, so an overhang as the light-shielding layer 3' in Fig. 8 is formed, or a taper is hardly formed as the light-shielding layer 3a in Fig. 8. And as shown in Fig. 11, when a flow of O_2 is further increased, the mask 4b formed of a photo resist shown in Fig. 8 is etched by the etching, so the taper angle decreases responding to the increase of the O_2

flow, and a taper such as the light-shielding layer 3b in Fig. 8 is formed.

[0085] So, in the present embodiment, as for the etching gas formed of $SF_6/CF_4/O_2$, in order that a taper is formed in the light-shielding layer 3 formed of WSi and a relatively high etching rate is obtained, a flow of SF_6 is set to be in a range of 5% to 30% of a flow of all the etching gases, a flow of CF_4 is set to be in a range of 30% to 75% of a flow of all the etching gases, and a flow of O_2 is set to be in a range of 20% to 40% of a flow of all the etching gases, as described above.

[0086] In this way, according to the present embodiment, as seen in Fig. 8 to Fig. 11, a practically reasonably high (that is, high to the extent that the etching depth can be controlled relatively easily) etching rate of approximately several hundred to several thousand Å/min can be obtained, while keeping uniformity of the etching rate in the surface to be etched. In addition, a practically moderate taper angle of approximately 80 to 50 degrees can be obtained.

[0087] After that, by the same processes as processes (2) to (10) of Fig. 6 and Fig. 7 described in the first example of the manufacturing process, a liquid crystal display panel 100 is manufactured.

[0088] By this manufacturing process, the first interlayer insulating layer 41, the TFT 30, the source electrode 35 (signal electrode), the gate electrode 31 (scanning electrode), pixel electrode 11, various wirings such as a wiring for the light-shielding layer 3 and the like are formed over the light-shielding layer 3 having a taper as a base, by processes (2) to (10). Therefore, adhesion of these interlayer insulating layer, the wiring or the like is dramatically good, compared to the case where a light-shielding layer in the shape of an overhang or a rectangle is used as a base, according to the above-mentioned conventional manufacturing technique, and as a result, a conduction failure such as breaking and an insulation failure between each layer are reduced.

[0089] Especially in the second example of the present manufacturing process, the gate electrode 31 (scanning electrode) may be formed from a WSi film with the same composition as the light-shielding layer 3, by the same sputtering process, photolithography process and etching process as the light-shielding layer 3 described above. In that case, as is the case with the light-shielding layer 3, when a wiring for electric connection to a driver circuit for X-side drive 101, the second interlayer insulating layer 42 and the like are formed over the gate electrode 31 (scanning electrode) as an example of a wiring having a taper, as a base, adhesion of these is dramatically good, which is an advantage.

[0090] As a result of the above, by the second example of the present manufacturing process, a liquid crystal display panel 100 which can display a well-colored,

high-definition image with a high contrast can be manufactured relatively easily.

[0091] <Third example of the manufacturing process> First, in the same way as the first example or the second example, a TFT array substrate 1 of a quartz substrate, hard glass or the like is prepared, as shown in the process (1) of Fig. 6.

[0092] Next, a light-shielding film is formed all over the surface of the TFT array substrate 1 by sputtering using a WSi target. Then, a mask which corresponds to a pattern of the light-shielding layer 3 is formed on the formed light-shielding film by photolithography. And by performing etching to the light-shielding film through the mask, the light-shielding film formed all over the substrate surface is left only in a region where a TFT 30 is to be formed, so that the light-shielding layer 3 is formed.

[0093] Especially in the third example of the manufacturing process, as is the case with the first example, in the sputtering process, a mole ratio (Si/W) of Si and W of the WSi target is in a range of 2.0 to 3.0, and the Si phase grain boundary size is 30 μm or less. And sputtering is performed so that the thickness of the light-shielding film is in a range of 1000 Å to 3000 Å.

[0094] Furthermore, especially in the third example of the manufacturing process, as is the case with the second example, in the etching process, $SF_6/CF_4/O_2$ are used as the etching gases for the chemical dry etching. And, a flow of SF_6 is set to be in a range of 5% to 30% of a flow of all the etching gases, a flow of CF_4 is set to be in a range of 30% to 75% of a flow of all the etching gases, and a flow of O_2 is set to be in a range of 20% to 40% of a flow of all the etching gases.

[0095] As a result of the above, a distortion and a crack can be prevented from being generated in the light-shielding layer 3, the TFT array substrate 1, the first interlayer insulating layer 41, each constituent element of the TFT 30 and the like, as is the case with the first example. In addition, characteristics deterioration of the TFT 30 caused by forming the light-shielding layer 3 under the TFT 30, a conduction failure and an insulation failure caused by forming the light-shielding layer 3 inside the base can be effectively prevented, as is the case with the second example.

[0096] As a result of the above, by the third example of the present manufacturing process, a liquid crystal display panel 100 which can display a well-colored, high-definition image with a high contrast can be manufactured relatively easily.

[0097] Lastly, consideration of how much the transistor characteristics of the TFT 30 are improved by a structure where the light-shielding layer 3 is formed by the sputtering process and the etching process unique to the present embodiment will be added, referring to Fig. 12 and Fig. 13. Fig. 12 shows the result of a transistor characteristics test for a liquid crystal display panel 100 of Fig. 1 manufactured by the third example of

the manufacturing process described above. Correspondingly, Fig. 13 shows the result of a transistor characteristics test for a comparative example where the light-shielding layer is formed of a Ti simple as an example of a refractory metal with the structure of the liquid crystal display panel 100 shown in Fig. 1. In Fig. 12 and Fig. 13, the horizontal axis shows a gate voltage applied to a gate electrode, and the vertical axis shows a drain current flowing at that time. In addition, the test results for two kinds of conditions, 15 V and 4 V as a source/drain voltage, are shown respectively.

[0098] Comparing Fig. 12 and Fig. 13, it is seen that the switching characteristics of the TFT is improved much better in the case where the light-shielding layer 3 is formed of WSi on the TFT array substrate 1 using the sputtering process and the etching process unique to the present embodiment, than the case where the light-shielding layer is formed of a Ti simple as an example of a refractory metal on the TFT array substrate 1.

[0099] In addition, in the case of the comparative example shown in Fig. 13, the switching characteristics of the TFT are improved, compared to the example of not providing a light-shielding layer at all and being affected by returning light directly.

[0100] The liquid crystal display panel 100 described above is applied to a color liquid crystal projector, so three liquid crystal display panels 100 are used as light valves for RGB respectively, and light of each color, decomposed through a dichroic mirror for RGB color decomposition, is entered into each panel as incident light. Therefore, in each embodiment, a color filter is not provided for the opposite substrate 2. However, in a liquid crystal display panel 100, color filters of RGB may be formed with the protective film on the opposite substrate 2 in a predetermined region opposing to the pixel electrode 11 where a black matrix 23 is not formed. By doing so, a liquid crystal display panel of the present embodiment can be applied to a color liquid crystal display device such as a direct-view-type or reflective color liquid crystal television, besides a liquid crystal projector.

[0101] Although, in the case of a liquid crystal display panel 100, incident light is entered from the opposite substrate 2 side in the same way as the conventional case, incident light may be entered from the TFT array substrate 1 side and exit from the opposite substrate 2 side, because the light-shielding layer 3 exists. That is, even when the liquid crystal display panel 100 is fixed to a liquid crystal projector in this way, light can be prevented from entering the p-Si layer 32 for channel formation, and a high-definition image can be displayed.

[0102] In the liquid crystal display panel 100, in order to control orientation defect of liquid crystal molecules in the TFT array substrate 1 side, a planarizing film may be further applied on the third interlayer insulating layer 43 by spin-coating or the like, or a

CMP treatment may be conducted.

[0103] In addition, although the description has been made setting that the switching element of the liquid crystal display panel 100 is a p-Si TFT of a positive stagger type or a coplanar type, application with various forms is possible even for a TFT of other types such as an inversely staggered TFT and an a-Si TFT, under a task of preventing returning light from entering a semiconductor layer for channel formation.

[0104] In addition, although the liquid crystal layer 50 is structured by nematic liquid crystal as an example in the liquid crystal display panel 100, polymer dispersion type liquid crystal where liquid crystal is dispersed as small particles in polymer may be used. In that case, orientation films 12 and 22, the above-described polarizing film, polarizing plate and the like become unnecessary, and advantages such as higher intensity and lower power consumption of the liquid crystal display panel due to increased usability of light can be obtained. Furthermore, in the case where the liquid crystal display panel 100 is applied to a reflective liquid crystal display device by structuring the pixel electrode 11 by a metal film with high reflectivity such as Al, SH (super homeotropic) liquid crystal in which liquid crystal molecules are aligned substantially vertical under the condition where no voltage is applied or the like may be used. Furthermore, although the common electrode 21 is provided on the opposite substrate 2 side so as to apply an electric field vertical to the liquid crystal layer 50 (longitudinal electric field) in the liquid crystal display panel 100, it is also possible to structure the pixel electrode 11 by a pair of electrodes for horizontal electric field generation respectively so as to apply an electric field parallel to the liquid crystal layer 50 (horizontal electric field) (that is, an electrode for longitudinal electric field generation is not provided on the opposite substrate 2 side, and an electrode for horizontal electric field generation is provided on the TFT array substrate 1 side). Using a horizontal electric field as this is more advantageous to widening the viewing angle, than using a longitudinal electric field. Besides the above, the present embodiment can be applied to various liquid crystal materials (liquid crystal phase), operation mode, liquid crystal alignment, driving method and the like.

[0105]

[Effects of the Invention] According to the manufacturing method of a liquid crystal display panel according to claim 1, the thermal compatibility between a light-shielding layer and a first substrate becomes good, and homogenization of film quality of the light-shielding layer is promoted. In addition, planarization of the upper surface of the light-shielding layer is promoted. In this way, stress does not excessively increase with the thickness of the light-shielding layer, so that a liquid crystal display panel with

enough light-shielding properties while preventing a distortion and a crack generated in the light-shielding layer, the first substrate, the interlayer insulating layer, each constituent element of the switching element or the like can be manufactured.

[0106] According to the manufacturing method of a liquid crystal display panel according to claim 2, a light-shielding layer having a taper can be formed by etching with a high etching rate, and an interlayer insulating layer, various wiring and the like can be formed thereon with good adhesion. Therefore, a liquid crystal display panel with enough light-shielding properties can be manufactured, neither deteriorating characteristics of the switching element since the light-shielding layer is formed under the switching element, nor causing a conduction failure or an insulation failure in the interlayer insulating layer, various wirings and the like since the light-shielding layer is formed inside the base.

[0107] According to the manufacturing method according to claim 3, since the sputtering process of claim 1 and the etching process of claim 2 are included, effects of these processes can be both obtained.

[0108] According to the manufacturing method of a liquid crystal display panel according to claim 4, even a wiring made of WSi such as a gate wiring can be formed so as to have a taper by etching with a high etching rate, in the same way as the case of the light-shielding film in claim 2 or 3, and various electrodes, an insulating layer, various wirings and the like can be formed thereon with good adhesion. Therefore, yield in manufacture of a liquid crystal display panel can be improved.

[Brief Description of the Drawings]

Fig. 1 is a cross-sectional view showing a structure of a liquid crystal display panel of the embodiment.

Fig. 2 is a plan view of a TFT array substrate structuring the liquid crystal display panel in Fig. 1.

Fig. 3 is a cross-sectional view of a storage capacitor structuring the liquid crystal display panel in Fig. 1.

Fig. 4 is a plan view showing the overall structure of the liquid crystal display panel in Fig. 1.

Fig. 5 is a cross-sectional view showing the overall structure of the liquid crystal display panel in Fig. 1.

Fig. 6 is a process drawing (1) showing the manufacturing process of the liquid crystal display panel in Fig. 1 in order.

Fig. 7 is a process drawing (2) showing the manufacturing process of the liquid crystal display panel in Fig. 1 in order.

Fig. 8 is a schematic diagram showing the relation between the overhang and a taper of a light-shielding layer and O_2 flow in the etching gas.

Fig. 9 is a schematic diagram showing change in the etching rate and change in uniformity for a light-shielding film in the manufacturing process of the present embodiment.

Fig. 10 is a characteristic diagram showing change in the etching rate for a quartz substrate in the manufacturing process of the present embodiment.

Fig. 11 is a characteristic diagram showing change in the etching rate and the taper angle for a light-shielding film in the manufacturing process of the present embodiment.

Fig. 12 is a characteristic diagram showing characteristics of a TFT provided for a liquid crystal display panel of the present embodiment.

Fig. 13 is a characteristic diagram showing characteristics of a TFT provided for a liquid crystal display panel as a comparative example.

[Description of Symbols]

1: TFT array substrate

2: opposite substrate

3, 3a, 3b and 3': light-shielding layer

4a, 4b and 4': mask

11: pixel electrode

12: orientation film

21: common electrode

22: orientation film

23: black matrix

30: TFT

31: gate electrode

32: p-Si layer

33: gate insulating layer

34: source region

35: source electrode (signal electrode)

36: drain region

37 and 38: contact hole

41: first interlayer insulating layer

42: second interlayer insulating layer

43: third interlayer insulating layer

50: liquid crystal layer

52: sealing agent
70: storage capacitor
100: liquid crystal display panel
101: driver circuit for X-side drive
102: mounting terminal
104: driver circuit for Y-side drive

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